UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/955,076	09/19/2001	Eiji Sakagami	214019US2	9771

22850 7590 06/13/2005

OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
WEISS, HOWARD	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/955,076	SAKAGAMI, EIJI
	Examiner	Art Unit
	Howard Weiss	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *7-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-21* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Attorney's Docket Number: 214019US2

Filing Date: 9/19/01

Continuing Data: RCE established 5/8/03, 4/26/04 and 5/2/05

Claimed Foreign Priority Date: 9/21/00 (JPX)

Applicant(s): Sakagami

Examiner: Howard Weiss

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/2/05 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 to 3, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fang (U.S. Patent No. 6,023,085), Reisinger (U.S. Patent No. 6,137,718), Pradeep et al. (U.S. Patent No. 6,228,713) and Jang et al. (U.S. Patent No. 5,786,262).

Fang shows most aspects of the instant invention (e.g. Figures 7 and 9) including:

- a semiconductor substrate **304** with a cell array formed in a well **305** (Column 9 Lines 16 to 23)

- a first cell transistor **346** including a first gate insulating film **308**, a charge storage layer **316a** and a first gate electrode **338** said charge storage layer existing only below the first gate electrode
- a second selection transistor **344** adjacent to said first cell transistor and including a second gate insulating film **336** and a second gate electrode **338** laterally separate from the first gate electrode
- peripheral transistors **332, 342** with gate electrodes **338** and gate insulting films **337,336** of different thicknesses

Ogura et al. do not show the first and second transistor isolated by a trench, a bottom insulating film formed on the trench inner surface and an insulating layer filling said trench on said bottom insulating layer, said first gate insulating film comprising a silicon oxide/silicon nitride/silicon oxide (ONO) multi-film structure with the silicon nitride film as said charge storage layer, a height of the charge storage layer above the substrate lower than a height of the material filling said trench, the width of the charge storage layer corresponding to a width of the element region and a thickness of the bottom insulating film and a height of the second gate insulating film in said second transistor is lower than a height of the insulating film and is lower than a height of the first gate insulating film.

Reisinger teaches (e.g. Figure 1 and Column 5 Lines 45 to 56) to form an ONO gate insulating layer **5** with a silicon nitride layer **52** as a charge storage layer, the thicknesses of said layers within the claimed ranges and the thickness of the bottom oxide layer **51** smaller than the top oxide layer **53** and a height (i.e. thickness) of the second gate insulating film (i.e. 16 nm; see Figure 7B in Fang) in said second transistor is lower than a height of the insulating film (see Pradeep next paragraph) and is lower than a height of the first gate insulating film (i.e. at maximum 20.5 nm; see Column 5 Lines 46 to 56 in Reisinger) to increase storage density and data retention (Column 2 Lines 7 to 12). It would have been obvious to a person of ordinary skill in the art at the time of invention to form an ONO gate insulating layer

with a silicon nitride layer as a charge storage layer, the thicknesses within the claimed ranges, the thickness of the bottom oxide layer is smaller than the top oxide layer and a height of the second gate insulating film in said second transistor is lower than a height of the insulating film and is lower than a height of the first gate insulating film as taught by Reisinger in the device of Fang to increase storage density and data retention.

Pradeep et al. teach (e.g. Figure 7A) to isolate memory cells with trench isolations **24** in element isolation regions with the charge storage layer **14** with a height lower than the trench isolations and restricted from said element isolation regions to reduce the masking and etching steps and create a self-aligned structure (Column 1 Lines 49 to 53). It would have been obvious to a person of ordinary skill in the art at the time of invention to isolate memory cells with trench isolations in element isolation regions with the charge storage layer with a height lower than the trench isolations and restricted from said element isolation regions as taught by Pradeep et al. in the device of Fang to reduce the masking and etching steps and create a self-aligned structure.

Jang et al. teach (e.g. Figure 10) to form a bottom insulating layer **14** in a trench's inner surface **10** (Figure 8) to provide better isolation (Column 4 Lines 31 to 38). The Examiner notes that the position of the bottom insulating layer of Jang et al. when combined with the features of the prior art above, the width of the charge storage layer will correspond to a width of an element region and a thickness of the bottom insulating film. It would have been obvious to a person of ordinary skill in the art at the time of invention to form a bottom insulating layer in a trench's inner surface so the width of the charge storage layer will correspond to a width of an element region and a thickness of the bottom insulating film as taught by Jang et al. in the device of Fang to provide better isolation.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fang, Pradeep et al., Jang et al. and Reisinger, as applied to Claim 1 above, and further in view of Agarwal et al. (U.S. Patent No. 6,201,276)

Fang, Pradeep et al., Jang et al. and Reisinger disclose the claimed invention (Paragraph 3) except that the charge storage layer comprising either a silicon nitride or a tantalum oxide film instead of either a strontium titanate or a barium strontium titanate film. Agarwal et al. teach (Column 4 Lines 33 to 36) that either a strontium titinate or a barium strontium titanate film are equivalent structure known in the art. Therefore, because these charge storage films were art-recognized equivalents at the time the invention was made, one of ordinary skill in the art would have found it obvious to substitute either silicon nitride or tantalum oxide for strontium titinate or barium strontium titanate.

Response to Arguments

5. Applicant's arguments filed 10/22/04 have been fully considered but they are not persuasive. The Applicant outlines four (4) features, labeled (a) to (d), which are allegedly not disclosed by the combination of the prior art. The Examiner will address where each of these features are disclosed:

(a) Fang specifically states that the cell array is formed in a well **305** (Column 9 Lines 16 to 23);

(b) The Applicant incorrectly states that the second gate insulating film in the second transistor has bottom and top gate insulating films when the claims specifically state that the first gate insulating film of the first transistor has this structure. After incorporating the ONO charge storage gate dielectric of Reisinger, the structure of the first transistors of Fang (Figure 7A) would be changed so that the tunnel oxide and the Poly 1 layers of Fang would be eliminated. Both oxide layers permit charge to pass into the charge storage nitride layer (see Column 4 Lines 12 to 26 of Reisinger)

(c) The height of the first insulating film **30** would be lower than the insulating film **24** as shown in Figure 7A of Pradeep et al. (remember, there would be only an ONO first insulating film). If the height of the second gate insulating film is less than the first gate insulating film, then is follows that the second gate insulating film would be lower then the insulating film

(d) The height of the second gate insulating film is 16 nm (see Figure 7B of Fang). The maximum height of the ONO first gate insulating film is 20.5 nm (6 nm + 8 nm + 6.5 nm; see Column 5 Lines 46 to 56 in Reisinger) and would be higher.

In view of these reasons and those set forth in the present office action, the rejections of the stated claims stand.

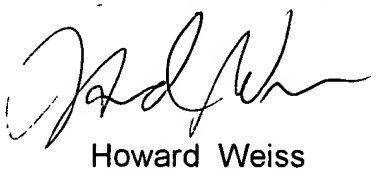
Conclusion

6. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 872-9306**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Howard Weiss at **(571) 272-1720** and between the hours of 7:00 AM to 3:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via **Howard.Weiss@uspto.gov**. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on **(571) 272-1705**.

8. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/ 324,326	thru 6/9/05
Other Documentation: none	
Electronic Database(s): EAST	thru 6/9/05



Howard Weiss
Primary Examiner
Art Unit 2814

HW/hw
10 June 2005